Fractional Order PLL
Integer Order PLL (PLL) and Fractional Order PLL (FPLL)

A FPLL can be obtained by replacing normal capacitor of LF and/or VCO by FC.
**Fractional Phase Locked Loop**

- **Transfer functions of Loop filter**
  \[ T_{LF} = \frac{V_O(s)}{V_i(s)} = \frac{K_f}{S^\alpha + b} \]
  Where, \( K_f \) is the sensitivity of loop filter, \( \alpha \) is its order and \( b = \frac{1}{R_i C_F} \)

- **Transfer functions of VCO**
  \[ T_{VCO} = \frac{V_O(s)}{V_i(s)} = \frac{K_O}{S^\beta} \]
  Where, \( K_O \) is the sensitivity of VCO, \( \beta \) is its order

- **Transfer functions that relates phase error of FPLL**
  \[ \frac{\theta_e}{\theta_i} = \frac{S^\beta (S^\alpha + b)}{S^{\alpha+\beta} + bS^\beta + K} \]

- **The input signal phase and VCO output phase can be expressed as**
  \[ \frac{\theta_o}{\theta_i} = \frac{K}{S^{\alpha+\beta} + bS^\beta + K} \]
  Where, \( K_d \) is the sensitivity of PD and \( K = K_f K_o K_d \)

  The FPLL shows a fractional order low pass response from where the different performances are measured

For simulation, \( b = 2.77 \times 10^3 \)  \( K = 7.25 \times 10^6 \)
Circuit Diagram of FPLL
Realization of FPLL through Experimentation

FPLL has been realized with two FCs for two center frequency, i.e, 935 Hz and 12 kHz

To realize FPLL, the capacitor (C) replaced with FC in PLL

The $f_0$ is changed by changing the external parameter $R_o$ and $C_o$ as $f_0 = 0.3/(R_o C_o)$

$C_{F31}$ is used for $f_0 = 935$ Hz and $C_{F32}$ is used for $f_0 = 12$ kHz.

The $\alpha$ is changed from 0.43 to 0.36 when $f_0$ is changed from 935 Hz to 12 kHz, but $\beta$ remain constant ($\beta=1$)

The capture range and bandwidth increases as compared to an IPLL and lock range remains constant
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<table>
<thead>
<tr>
<th>Components used</th>
<th>Component values for $f_o = 935$ Hz</th>
<th>Component values for $f_o = 12$ kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R$</td>
<td>0.68 kΩ</td>
<td>0.68 kΩ</td>
</tr>
<tr>
<td>$C_{in}$</td>
<td>$0.2 \times 10^{-6}$ F</td>
<td>$0.2 \times 10^{-6}$ F</td>
</tr>
<tr>
<td>$R_0$</td>
<td>9.71 kΩ</td>
<td>25 kΩ</td>
</tr>
<tr>
<td>$C_0$</td>
<td>$33 \times 10^{-9}$ F</td>
<td>$1 \times 10^{-9}$ F</td>
</tr>
<tr>
<td>$C_{F31}$</td>
<td>$0.103 \times 10^{-6}[F/s^{0.57}]$</td>
<td>$-$</td>
</tr>
<tr>
<td>$C_{F32}$</td>
<td>$-$</td>
<td>$1.06 \times 10^{-7}[F/s^{0.64}]$</td>
</tr>
<tr>
<td>$b_2$</td>
<td>$2.77 \times 10^{3}$</td>
<td>$2.85 \times 10^{3}$</td>
</tr>
<tr>
<td>$\alpha$</td>
<td>0.43</td>
<td>0.36</td>
</tr>
<tr>
<td>$\beta$</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>loop gain ($K$)</td>
<td>$7.25 \times 10^{6}$</td>
<td>$1.12 \times 10^{8}$</td>
</tr>
</tbody>
</table>

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Performance Study of FPLL

Capture range increases with decrease in loop filter order ($\alpha$) i.e., from 657 to 820 Hz when order ($\alpha$) changes from 1 to 0.1

Lock Range ($\pm \Delta \omega_l$)

The range of frequency over which the loop can track the input, once lock has been established, is called lock range.

Lock range is independent of order of $\alpha$

Lock range of FPLL is same as PLL for condition $0 < \alpha < 1$, $\beta = 1$

Lock time (time taken for the transients of step response to die out) reduces.
Transient Response of FPLL

For simulation
\[ b = 2.77 \times 10^3, \]
\[ K = 7.25 \times 10^6 \]

Transient response of PLL (a) VCO output  
(b) PD output

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Summary

• Experimental validation of FPLL for two center frequency i.e, 935 Hz and 12 kHz

• Compared to PLL, a FPLL has
  - Larger bandwidth
  - Less locking time,
  - Higher capture range

FPLL loop waveforms:
Top: Input signal,
Middle: VCO output,
Bottom: Voltage across $C_0$
Performance of FPLL

**Bandwidth:** The bandwidth of FPLL can be simulated from the following Eqn.

\[ \omega^{2(\alpha + \beta)} + x\omega^{\alpha + 2\beta} + y\omega^{\alpha + \beta} + z\omega^\beta + b^2\omega^{2\beta} - K^2 = 0 \]

Where,

\[ x = 2b \cos \frac{\pi \alpha}{2} \]
\[ y = 2K \cos \frac{\pi (\alpha + \beta)}{2} \]
\[ z = 2bK \cos \frac{\pi \beta}{2} \]

Bandwidth can be increased by decreasing both \( \beta \) and \( \alpha \)

Increase in Bandwidth make FPLL vulnerable to noisy signal

**Capture Range \( (\pm \Delta \omega_c) \)**

- The capture range is the frequency range \( \pm \Delta \omega_c \), centered about \( \omega_o \), over which the loop can acquire lock. The capture range of FPLL for \( 0 < \alpha < 1, \beta = 1 \)

\[ \Delta \omega_c^{2+2\alpha} + 2b\Delta \omega_c^{2+\alpha} \cos \frac{\pi \alpha}{2} + b^2\Delta \omega_c^2 - K^2 = 0 \]
On-line tunable fractional order resonator and filter
Fractional order series resonator

- Theoretically proved that infinite Q factor can be achieved
- In practice Q factor was 102 to 326
- Has same frequency for minimum impedance and zero phase
- Successfully tune in the implemented hardware circuit
- The FOE exponent $\alpha, \beta$ does not take part in tuning
- Increases he designer's degree of freedom

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A Adhikary, S Sen, Karabi Biswas, “Design and hardware realization of a tunable fractional-order series resonator with high quality factor” Circuits, Systems, and Signal Processing 36 (9), 3457-3476
The beginning

○ 1695: Conversation between L’Hopital and Leibniz about the nth-derivative of the linear function

\[ f(x) = x^n \frac{d^n x}{dx^n} \]

○ Interest on such behaviour in mathematics was reflected by the work of Riemann, Liouville, Gruinwald and Letnikov, and some other mathematician

○ The mathematical work culminated with the book published by Oldham and Spanier in 1974

History of development

- On a parallel track, interest on non-integer order control began in the middle of 20th century.

- 1945: Bode implemented a desired 60 degree phase control circuit using 19 elements (did not mention the term fractional).

  - Coincidentally in 1941 Cole and Cole discovered the power law behaviour of different materials.

  - The behaviour was termed as Constant Phase Element (CPE).

  - In last 75 years, numerous techniques were adopted to realize FOE, broadly classified as:
    - Multi component FOE
    - Single component FOE

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Multi component FOE

- **1950**: Darlington used pair of phase shifting networks for approximation and realization of constant phase difference
  - Required inductors and capacitors and not suitable for circuit application

- **1960**: Manabe used the idea of non-integer order control to stabilize autonomous flight dynamics

- **1961**: Douglas realized CP functions cascading R-C block
  - The design had defined design technique for achieving desired CP, CP zone and phase ripple.

- **1963**: Lerner made the realization simpler by putting only RC parallel in each block
  - It introduces impedance compensation to reduce phase error at the boundaries of CP zone

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Multi component realization

- 1964: Carlson and Halijak generalized the pole placement process by regular Newtonian process
  - This established the physically realizability of a truncated ladder
  - But it required arbitrary resistors and capacitors

- 1966: The limitation was partially overcome by S. C. Dutta Roy by offering two schemes for realization
  - Identical T network
  - Identical parallel RC network

\[ \alpha = 0.5 \text{ only realizable} \]
Multi component realization

- **1983**: Oldham adopted truncated ladder structure to realize FOE
  - Defied guideline to achieve any value of $\alpha$
  - $R$ and $C$ are in geometric progression.

- **1990**: The connection between mathematics and physical properties of material established

- **1999**: Igor Podlubny had included the concept of fractional order control design

- Rational approximation was extensively used for realizing the fractional operator
Multi component realization

- 2005: Charef proposed GIC based inductive FOE

- 2013: At IIT Kharagpur- Khanra et. al proposed realization of $Ks^\alpha$, where $\alpha$ can be any real number

The above realization mainly dealt with the

- Exponent $\alpha$
- Constant Phase Zone
- Phase ripple

No definite guideline to design the coefficient $Z$
Realization of fractional order system through transfer function

\[ \text{Pole } = 1/(s+1/R_f C_f), \text{ Zero } = S+1/R_i C_i \]

Different circuits to get the Pole Zero pair

Munmun Khanra, Jayanta Pal and Karabi Biswas; Rational approximation and analog realization of fractional order transfer function with multiple fractional powered terms, Asian Journal of Control, Vol. 15, No. 3, 2013
Prime Issues to be addressed

**ISSUES**

- Standardization of development process of FOE
- Meeting pre-defined specifications
- Proper packaging ensuing small sized and long life.

- Improvement of **longevity**

**CHALLENGES**

- To understand how and why CP is generated.
- To model the system with physically and chemically significant electrical parameter.
- To explore new type of metal-polymer-electrolyte interface.

- Get rid of the **drift in the behaviour** over time.
- Replacement by **semi-solid electrolyte** without deviating behaviour.
Summary

1. Analysis of origin of fractance
2. Control on the origin of fractance
3. Develop a commercially viable element to be used in circuit

4. Low cost, portable, moderately accurate chemical sensor
   a. Detection of milk adulteration
   b. Detection of urea in blood and urine
   c. Detection of urea in land water and sewage
   d. Quality control of beverages, tea

5. Develop new signal processing circuit
   a. FO Integrator,
   b. FO Differentiator,
   c. FO Biquad Filter,
   d. FO based PLL

6. Develop new robust controller

The fourth element in electrical engineering apart from resistor, inductor and capacitor

Domestic Application
Clinical Application
Environmental Application
Business Application
Essential tools

Fractional calculus

Fractional order element
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Thank you for your attention